LAB 2 Basic CMOS Amplifiers

I. Objective

Design, simulate, and prototype the common source and source follower amplifiers.

II. Preparation

Basic Concepts

The input-output characteristic of an amplifier is generally a non-linear function that can be approximated by a polynomial over some signal range:

$$y(t) \approx a_0 + a_1 x(t) + a_2 x(t)^2 + \ldots + a_n x(t)^n, \qquad x_1 \le x \le x_2 \qquad (1)$$

The input, x(t), and output, y(t), may be current or voltage quantities. For a sufficiently narrow range of x the circuit can be modeled as a linear amplifier:

$$y(t) \approx a_0 + a_1 x(t), \qquad (2)$$

where a_0 is the operating (bias) point and a_1 is the small-signal gain. It is under this assumption that we perform small-signal analysis on transistor circuits using models such as the hybrid-π or T-model. Operating points of transistors are set by on-chip biasing networks or off-chip DC signals. As the input x(t) increases in magnitude however, higher order terms manifest themselves in the input-output characteristic, as seen in Equation (1), leading to nonlinearity and necessitating large-signal analysis.

Typical performance metrics for an amplifier include gain, bandwidth, slew rate, linearity, noise, dynamic range, power dissipation and supply voltage. Furthermore, input and output impedances determine how the circuit interacts with the preceding and subsequent stages. In practice, most of these parameters trade off with each other, making the design a multi-dimensional optimization problem. The purpose of this lab is to investigate and understand some of these trade-offs by analyzing the impact of different bias conditions on the small-signal performance of two single-stage amplifiers: (a) the common source (CS) amplifier, and (b) the source follower (SF). The instructions that follow will guide you through the steps of hand analysis, simulation and prototyping of these circuits. In lab 2, the intuition gained in this exercise will help you to design an operational amplifier circuit.

In your designs you will again use the commercially available MOS transistor bank chips of 4007 series. Their pinout is given in the datasheet posted on the course website. For both

designs, use a 10V voltage supply , and the de vice parameters from T able 1 for your hand calculations.

Table 1: 4007 CMOS Device Parameters

Parameter	NMOS	PMOS
Vt_0 (V)	1.77	-1.40
K (= μC_{ox} A/V^2)	2.17e-4	3.20e-5
γ (V$^{1/2}$)	1.85	3.30
λ	0.64e-2	5.7e-2
W/L	4	20
C_{gs}	18 pF	17pF
C_{gd}	14 pF	26 pF

a) Common Source Amplifier

Design an n-channel common source amplifier as shown below (Fig 3.5 of the textbook).

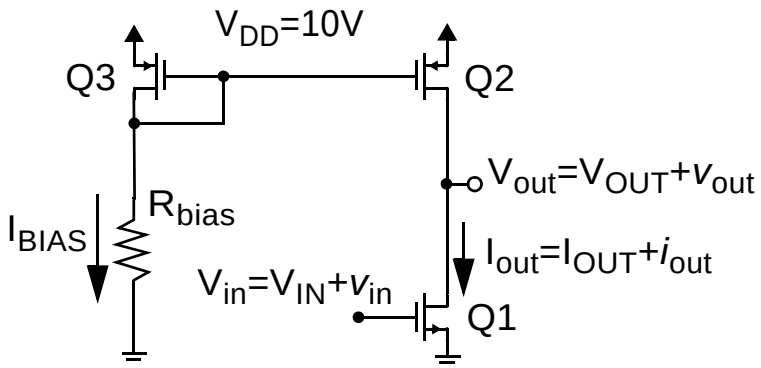

Figure 1: Common source (CS) amplifier.

Circuit Description

The first step in the analy sis of an analog circuit is identifying the biasing network and the signal path. In this simple circuit, Q1 acts as the amplifier and Q2, Q3 and R_{bias} make up the biasing network. The operati ng point of the CS amplif ier is defined by the following quiescent voltage and current signals as labeled in Fig. 1: V_{IN}, V_{OUT}, I_{OUT} and V_{DD}. In the lab, V_{IN} and V_{DD} are off-chip DC voltage signals. I_{OUT} is generated by the p-channel current mirror in order to define the drain current of transistor Q1. Notice that Q2, in addition to setting the drain current I_{OUT}, acts as an active load. The benefit over a resistive load is that a higher output impedance is achieved.

The aforementioned DC biasing signals set the small-signal parameters of the CS amplifier, including the transconductance of Q1 (g_m) and the output impedance of the circuit (r_{out}). Once the operating point has been defined, the AC operation of the CS amplifier can be analyzed. Transistor Q1 converts small-signal variations in its gate-source voltage (v_{in}) to a small-signal drain current, i_{out}, as set by its transconductance, g_m. This small-signal drain current passes through the output impedance of the CS amplifier, r_{out}, and generates a small-signal output voltage, v_{out}, that is added to the DC component of the output, V_{OUT}. As you can see, the biasing conditions dictate how well the CS amplifier will perform.

Hand Analysis

DC Analysis

1. Determine the DC drain currents (I_{OUT}) required to bias transistor Q1 with effective voltages of 400mV and 1V. Do not ignore channel length modulation.

   HINT: Choose $V_{DS1}=V_{DD}/2$ for the maximum output voltage swing.

2. Design two current mirrors, consisting of Q2, Q3 and R_{bias}, with the transistor ratio of 1:1 to generate the bias currents calculated in item 1 above.

3. Calculate the output impedance of the amplifier under each biasing condition.

AC Analysis

The AC design of an amplifier involves sizing and biasing transistors in the signal path, in this case Q1. Because in this lab sizes of discrete components are fixed and biasing conditions are given, we proceed directly to characterize the small-signal performance of the amplifier. For each biasing condition (V_{eff}=400mV and V_{eff}=1V) calculate the following small-signal performance metrics:

- gain (dB)
- bandwidth (Hz)
- unity-gain frequency (Hz)

Transient Analysis

Estimate the slew rate (V/ μs) of your amplifier under each biasing condition. Is this circuit limited by the positive or negative slew rate? Why?

HSPICE Simulation

You will now verify the calculated performance of the amplifier under two biasing conditions by simulating it with HSPICE. Use the models provided on the course website. Summarize all of your calculated and simulated results in a table and comment on any differences.

DC Simulations

Run a DC operating point simulation. In the lab, not all resistance values are available. Using the closest available resistor value listed in Appendix G of reference [2], simulate and refine your current mirror designs to ensure that in each amplifier, Q1 is biased with V_{eff}=0.4V and V_{eff}=1V respectively. Draw the circuit you will use to measure the output resistance in the lab and verify its functionality in simulation. How do the DC operating points and the output impedances of the amplifier compare with your calculations?

AC Simulations

Generate the Bode plots for the amplifier in order to fully characterize its frequency response. Compare the simulated versus calculated midband gain (dB), bandwidth (Hz) and unity gain bandwidth (Hz).

Transient Simulations

Using a square wave input, simulate the amplifier's slew rate for each biasing condition and compare with your calculations.

b) Source Follower

Design an n-channel source follower (SF) as shown in Figure 2 (Fig. 3.6 of the textbook).

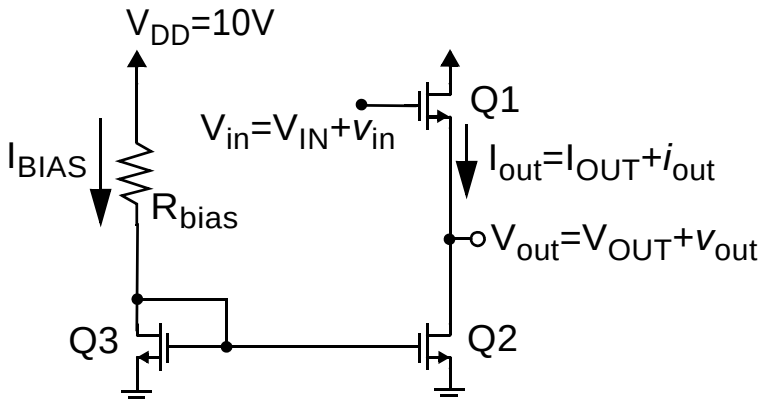

Figure 2: Source follower (SF).

Again, use effective voltages of 400mV and 1V, and a 10V supply. Follow the same design procedure outlined within the '**Hand Analysis'** and '**HPSICE Simulation'** sections in part (a). Summarize all of your calculated and simulated DC, AC and transient analysis results in a table and comment on any differences.

III. Experiment

1. Build a single n- and p-channel current mirror, changing bias resistors to realize different bias currents. Measure the output currents. Measure the output resistances using the test circuit you devised in the '**Preparation'** section.

2. Wire up the common source and source follower amplifiers. Choosing **one** of your designs (i.e., either V_{eff}=400mV or 1V), perform the following measurements on the completed circuits:

Common Source Amplifier:

- DC gain
- Bandwidth
- Unity-gain frequency
- Slew rate

Source Follower:

- DC gain with and without body effect
- Bandwidth
- Output resistance
- Slew rate

Present your final measured results to the TA at the end of the lab. Be prepared to discuss your measured results in relation with your calculated and simulated results.

References

[1] A. Chan Carusone, D. Johns and K. Martin, *Analog Integrated Circuit Design*, Wiley, 2011.

[2] A.S. Sedra and K.C. Smith, *Microelectronic Circuits 5th Edition*, Oxford University Press, 2004.

[3] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw Hill, 2001.