LAB 4 A Folded-Cascode Operational Amplifier

I. Objective

Design, simulate, and prototype the CMOS operational amplifier in Figure 1 using discrete MOSFETs to satisfy the specifications listed below. Use the design methodology as detailed in the subsequent sections. You will need to select values for R_b and V_C. You may also vary the effective widths of the MOSFETs by placing multiple devices in parallel. Be prepared to justify your design choices. Use the device parameters provided in the previous lab for your hand calculations.

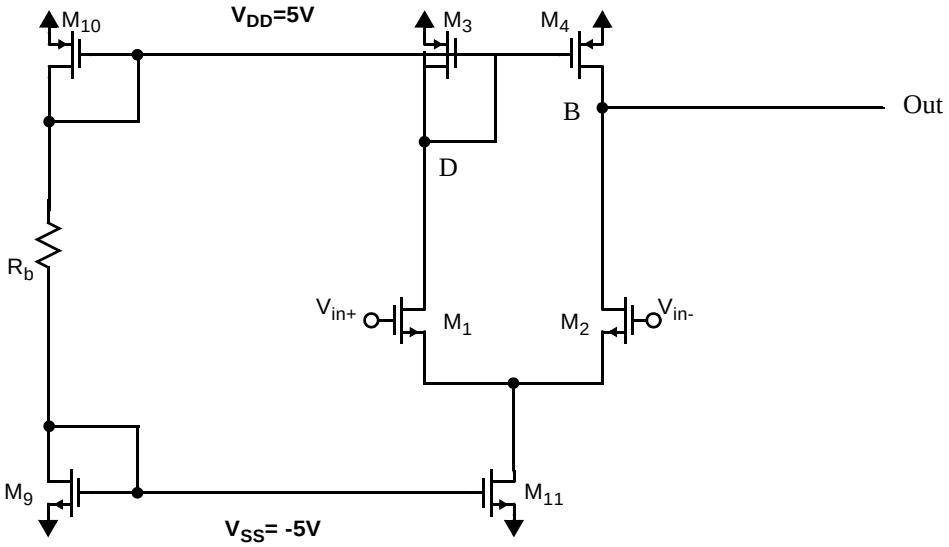


Figure 1: Folded-Cascode OpAmp

Parameter	Specification
DC Open Loop Gain	> 50 dB
Phase Margin ($\beta = 1$)	> 60 degrees
Slew Rate	$\pm 2V/\mu$sec
Unity gain bandwidth	500 kHz
Capacitive load, C_L	100 pF

II. Preparation

Hand Analysis: Design Methodology

The first step is to understand how the folded cascode op amp works. Read section 6.4 of the course textbook. The design methodology for any transconductance amplifier is iterative. A general approach for the folded-cascode amplifier follows. Be sure to document your design procedure and equations in detail in your lab book. After running HSPICE simulations in the next section, you will be asked to substitute in simulated small signal parameters (ie. g_m, r_{ds}, etc...) back into your equations to arrive to more accurate estimates of your amplifier's performance.

a. Slew Rate

Because there is no power consumption specification (due to fixed sizes of discrete components) your design should begin by determining the minimum power dissipation and thus the minimum bias current. The necessary value for R_b can then be calculated. The minimum bias current required will be set by the slew rate specification. Be sure to include the effect of transistor parasitic capacitances at the critical output node when calculating your current.

b. Sizing

Because you are limited to fixed sizes of discrete components, you will need to determine which, if any, devices need to be placed in parallel. As discussed in the textbook, the critical size ratio to be determined is that of M1 to M5 (and M2 to M6). This should be done with consideration to the UGB set by the g_m of the input stage. Is one transistor enough or do you need more to reach the UGB specification?

c. Unity Gain Bandwidth (UGB)

A primary performance target for this folded-cascode amplifier design, and all opamps in fact, is to maximize its DC open loop gain as well as its performance when used in a feedback configuration. As a result, the open loop -3dB bandwidth is not a critical specification, and the unity gain bandwidth takes precedence. Calculate the UGB and confirm the choice of the bias current in section (a) and sizing in section (b).

d. DC Open Loop Gain

With the design choices you have made, calculate the open loop DC gain of your amplifier. Does it meet the specification or do you have to modify your design choices?

e. Phase Margin

Using open circuit time constant analysis, calculate the time constants at each of the four nodes in the signal path of the circuit. These are, in order of importance, nodes A, B, C and D as labelled in Figure 1. You now have sufficient information to calculate your expected -3dB

frequency and more importantly for compensation, your equivalent second pole frequency. Calculate your phase margin, and if needed, compensate your cascode amplifier so that it meets the phase margin specification.

f. Final Quiescent Bias Points

Once you've iterated through steps (a) to (e) above, calculate and label all bias voltages and currents on your circuit schematic diagram such that the output voltage swing is maximized. How will you bias the cascode transistors? How will you set your input common mode voltage?

HSPICE Simulation

1. Simulate your circuit using HSPICE and the 4007 series transistor bank transistor models provided on the course website. Summarize your calculated and simulated results in a table and comment on any differences. For your calculated results, be sure to re-calculate your gain, slew rate, bandwidth, unity gain bandwidth and phase margin using simulated parameter values for g_m and g_{ds} ($g_{ds}=1/r_{ds}$) for each MOSFET. This information can be found in your output ".lis" file generated by HSPICE. Include the following items in your lab book:

- AC open-loop frequency response curve (magnitude and phase) showing DC gain and phase margin assuming $\beta = 1$.
- The transient step response. Characterize the step response by applying a $1V_{pp}$ square wave to the op-amp in a non-inverting, unity-gain configuration. Measure the positive and negative slew rates.
- An estimate of the input-referred DC offset of your opamp yielding maximum output swing. Assume the input common-mode is at 0V.

2. Sketch the op-amp circuit at the chip level. Number each 4007 IC, label the pins of each IC, and show the wiring between the chips. This is a schematic diagram of your amplifier as it will look on your protoboard. Be sure to match both sides of the differential circuit. This means that if you have a differential pair, or two biasing transistors such as M3 and M4, make sure they are on the same chip. This will minimizes mismatches in your final design. As the only exception, choose M1 and M2 as the NMOS devices with pins 3, 4 and 5 on two different chips.

3. Build the opamp using a protoboard. You are required to have the entire circuit wired up, including ALL components, as part of your lab preparation.

III. Experiment

The following procedure assumes you have the entire amplifier wired and powered up, with the correct DC levels applied to the inputs and to the gates of the cascode transistors.You will need a multimeter, a function generator and a oscilloscope to proceed.

a. DC Characterization (This is the hardest part!)

1. Set up the multimeter with two banana-to-alligator clip cables, one for the negative terminal and one for the positive. Connect long prototyping wires to each alligator clip and use these wires to probe your circuit. This will make voltage and current measurements easier to perform.

2. Measure all of your bias currents and node voltages in three steps:

   (i) the bias circuitry (M9-M11) ,

   (ii) the differential pair and active load (M1-M4) and finally,

   (iii) the folded cascode and active load (M6-M10).

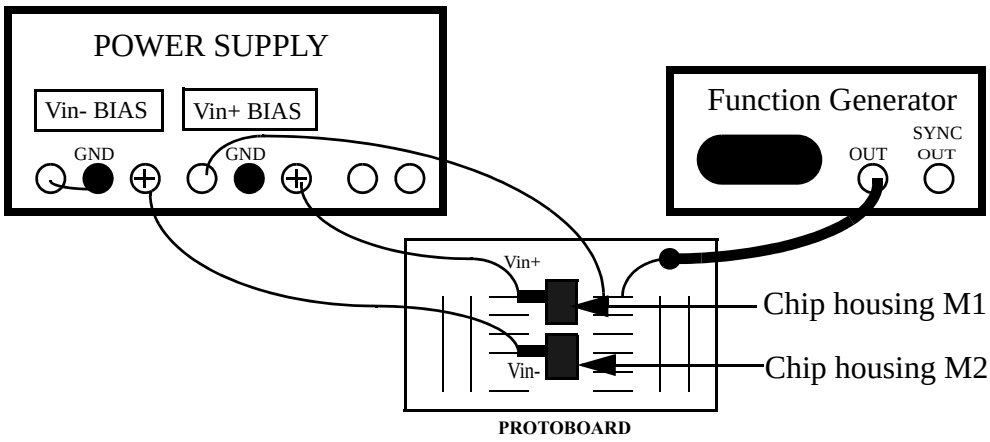
   - If your circuit is not biased properly, begin debugging your wiring one section at a time. Disconnect sections (ii) and (iii) and confirm that section (i) is working properly and continue on from there.

When you get to section (iii) at the output, note that your amplifier has extremely high gain and has an inherent offset. As a result, if your circuit is wired up correctly, your output node voltage will most likely be biased within a few hundred millivolts of your positive or negative supply.

3. The output voltage offset is due to input differential pair mismatch (input offset) and output current sources mismatch (systematic offset). Now that your circuit is biased, we must remove both offsets to maximize the output swing. Because the input-referred offset is on the order of millivolts, you will need to use the function generator (FG) as a high precision DC source in series with the common-mode input voltage set by the power supply.

   - Change the settings on the FG to “DC” and connect it to an unused pin/point on your board as shown below. Connect another wire from that point to the negative terminal of the DC power supply you are currently using to bias the non-inverting input terminal of your amplifier (Vin+). Be sure the negative terminal IS NOT connected to GND (you want to realize a series connection of two voltage sources). Now connect a

second wire from the positive terminal of the same supply to the inverting input terminal of your amplifier (Vin-). The final setup should look like this:



- Now you can compensate the output offset (on the order of millivolts).
- Connect the voltmeter across the terminals labelled A and C in Figure 1. Adjust the offset until the voltage drop V_A-V_C is zero. This is a very sensitive measurement. Record this input offset in your lab book. Now adjust the applied offset to center the output DC level for maximum swing.

b. AC Characterization

1. Measure the DC open-loop gain. You will do this via a single ended measurement. Begin by switching the FG from "DC" to "sinusoid". Note that no setup changes are required for this measurement. Use the FG to apply the necessary offset to achieve maximum output swing. Use the multimeter to verify this level.

2. Once you have the DC levels set for maximum swing, DISCONNECT THE MULTIMETER PROBES from your circuit. The multimeter may add substantial capacitance to the nodes it is probing and should never be connected during AC characterization. Measure and record the -3dB and unity gain bandwidth of your amplifier taking note of the following:
   - Set the oscilloscope to AC coupling on both Ch 1 and Ch 2.
   - Limit the BW of the scope (vertical menu button) to 20MHz
   - Be sure to set the scope to 'SAMPLE' mode in the "Acquire" menu when initially measuring your signals. Once you have a clean signal on Ch1 or Ch2, use this to trigger the scope. Apply averaging as required.
   - Measure the -3dB bandwidth with a very small signal (~20mV peak to peak). Ensure that no signals are clipping/slewing.
   - To measure the UGB, slowly increase the frequency of the signal source. Do not jump straight to higher frequencies. Furthermore, you may want to increase the amplitude of your input as you pass the -3dB point.

3. Connect the amplifier into a voltage follower configuration (notice that you do not need to change the connections to the function generator if you followed the procedure and connected it initially to the positive input Vin+). Measure the slew rate of your amplifier.

- Use a large step/square wave (8V peak to peak) at a very low frequency (~30Hz).

4. How do your measured results compare with the simulated results?

Present your final measured results to the TA at the end of the lab. Be prepared to discuss your measured results in relation with your calculated and simulated results.