LAB 1 MOS Device Parameters

I. Objective

Familiarize yourself with HSPICE and basic MOSFET model parameter extraction. Do this by running basic simulations and experiments upon individual NMOS and PMOS devices.

II. Preparation

Using HSPICE simulations,

1. Generate the following plots on linear scales for both NMOS & PMOS devices with $|V_{DS}| = 5V$:

- I_D vs. V_{GS}
- $\sqrt{I_D}$ vs. V_{GS}
- $\frac{dI_D}{dV_{GS}} = g_m$ vs. V_{GS}
- (g_m/I_D) vs. V_{GS}

Based on these simulations, what do you consider to be the threshold voltages of these devices? What is the value of $(W/L)\mu C_{ox}$?

How does this compare with the values reported in the simulator's dc operating point analysis?

2. For both the NMOS and PMOS device, with $|V_{GS}| = 5$ V constant, sweep V_{DS}. Plot I_D vs. V_{DS} and measure the slope of the curves when the transistors are in active mode. Estimate the model parameter λ for both the NMOS and PMOS device.

3. By simulation, attempt to determine the small-signal gate-source capacitance C_{gs} of both the NMOS and PMOS transistors when in active mode with $|V_{GS}| = |V_{DS}| = 5$ V.

HSPICE Simulation

Perform the preparation above using HSPICE and the 4007 device models provided on the course website. Summarize all of your calculated and simulated results in a table and comment on any differences.

III. Experiment

1. While keeping $|V_{DS}| = 5V$ constant, sweep V_{GS} to obtain a plot of I_D vs. V_{GS}, just as in the preparation. Based on these resuls, what do you consider to be the threshold voltages of these devices? What is the value of $(W/L)\mu C_{ox}$?

2. Perform an experiment in the lab that will allow you to estimate the small signal gate-source capacitance C_{gs} of individual NMOS and PMOS transistors when in saturation with $|V_{GS}| = |V_{DS}| = 5$ V.

Show the TAs your tabulated results for both the NMOS and PMOS devices, comparing the valus of threshold voltage, $(W/L)\mu C_{ox}$, and C_{gs} obtained in simulation and experimentally.