I. Objective

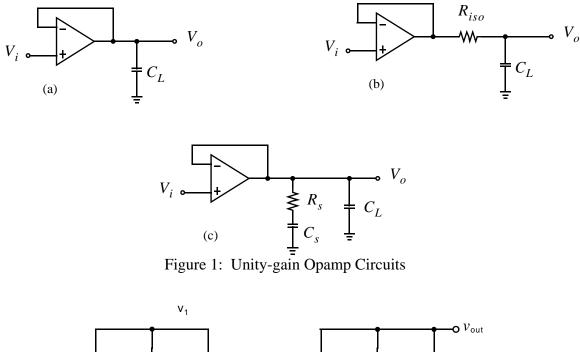
Learn some techniques to externally compensate an opamp driving large capacitive loads.

II. Preparation

Analysis

Assume the small-signal opamp model shown in Figure 2 where $\omega_{p1} = 1/(R_1C_1)$ is a dominant pole and ω_{p2} is at a much higher frequency.

1. For the circuit of Figure 1(a), find an expression for open-loop response L(s). Find an expression for the value of load capacitance C_L at which the opamp will exhibit 10%



 $g_{m1}v_{in}$ \downarrow R_1 \downarrow C_1 \downarrow $g_{m2}v_1$ \downarrow R_2 \downarrow C_2 \downarrow \downarrow

Figure 2: A simple small-signal model of the two-stage opamp.

overshoot. (The expression will be in terms of the opamp model parameters, g_{mi} , R_i , etc.) Sketch a Bode plot of the open-loop response in this case.

2. For the circuit of Figure 1(b), find an expression for open-loop response L(s). For the same value of C_L as in part 1, sketch a Bode plot of the open-loop response with R_{iso} in place. What is the effect of R_{iso} ?

For the circuit of Figure 1(c), find an expression for open-loop response L(s). For the 3. same value of C_L as in part 1, sketch a Bode plot of the open-loop response with R_s and C_s in place. What is the effect of R_s and C_s ?

HSPICE Simulation

1. Simulate the circuit of Figure 1(a) using HSPICE and the opamp model provided on the course website.

- Apply a step input at V_i of amplitude 100 mV and with $R_L = 2 \text{ k}\Omega$. Sweep C_L over a wide range and observe the resulting step responses at V_o . Produce plots of:

 - overshoot vs. C_L
 95% settling time vs. C_L
- Repeat part 1 for the circuit of Figure 1 (b). Use a value of $R_{iso} = 50 \ \Omega$. 2.
- Repeat part 1 for the circuit of Figure 1 (c). Use values of $R_s = 30 \ \Omega$ and $C_s = 5 \ nF$. 3.

You should have 6 plots in total. What was the effect of introducing the additional compensation components in Figures 1 (b) and (c) upon overshoot and settling time?

III. Experiment

1. Connect the circuits in Figures 1 (a) (b) and (c) in the lab reproduce the plots you obtained from simulation, this time measuring them experimentally. Use at least 10 different nicely-spaced values of load capacitance, C_L , to produce good plots. (Of course, you may connect multiple capacitors in parallel to do this.) Use the values for R_{iso} , R_s and C_s that were suggested in the preparation section.

2. How do your measured results compare with the simulated results?

Present your final measured results to the TA at the end of the lab. Be prepared to discuss your measured results in relation with your analysis and simulated results.